ing region **74**, **74'** are preferably formed epitaxially, in still additional embodiments, such regions may be part of an initial substrate in which devices **70**, **70'**, **95** are subsequently formed and one or both epitaxial deposition steps (e.g., EPI-1 and/or EPI-2) may be omitted. Still further, while in the preferred embodiment, N WELLs **761**, **762**, **761'**, **762'** are formed by multiple masking and implant steps, in other embodiments, such multiple masking and implant steps may be combined provided that the serially coupled ESD transistors in the ESD stack have different base-collector spacing dimensions D, with none or no more than one spacing dimension D chosen from zone Z**1** and others chosen from zones Z**2** and/or Z**3** of FIG. **5**, with the number depending upon the total number of stacked transistors being employed to achieve the desired value of $Vt1_{STACK}$. In further embodiments, DTI regions **792**, **792'** may be omitted and lateral isolation of ESD clamp transistors **70**, **70'**, etc., be provided by means of N WELLS **761**, **762**, etc., or equivalents. Either arrangement is useful.

[0046] According to a first embodiment, there is provided an ESD clamp (**21**), comprising, a first bipolar transistor (ESD-Z**1**) having a first emitter region (**78'**), a first collector region (**762'**), a first base region (**75'**) and a first base region to collector region spacing dimension D_{Z1}; and further is adapted to have a first trigger voltage $Vt1_{Z1}$ at $D=D_{Z1}$, a second bipolar transistor (ESD-Z**2** or ESD-Z**3**) series coupled to the first bipolar transistor (ESD-Z**1**) and having a second emitter region (**78**), a second collector region (**76**), a second base region (**75**) and a second base region to collector region spacing D_{Z2} or D_{Z3}; and further is adapted to have a second trigger voltage $Vt1_{Z2}$ or $Vt1_{Z3}$ different than the first trigger voltage $Vt1_{Z1}$, and wherein the first transistor (ESD-Z**1**) is adapted to have a slope $(\Delta Vt1/\Delta D)_{Z1}$ at $D=D_{Z1}$ and the second transistor (ESD-Z**2** or ESD-Z**3**) is adapted to have a slope $(\Delta Vt1/\Delta D)_{Z2}$ at $D=D_{Z2}$ or $(\Delta Vt1/\Delta D)_{Z3}$ at $D=D_{Z3}$, and wherein $(\Delta Vt1/\Delta D)_{Z1}$ is greater than $(\Delta Vt1/\Delta D)_{Z2}$ or $(\Delta Vt1/\Delta D)_{Z3}$. According to a further embodiment, D_{Z2} is less than D_{Z1}. According to a still further embodiment, the second transistor (ESD-Z**2**) has a second spacing D_{Z2} and is adapted to have a trigger voltage $Vt1_{Z2}$ and slope $(\Delta Vt1/\Delta D)_{Z2}$ at $D=D_{Z2}$, wherein the clamp (**21**) further comprises, a third bipolar transistor (ESD-Z**3**) serially coupled to the first bipolar transistor (ESD-Z**1**) and the second bipolar transistor (ESD-Z**2**) and having a third emitter region (**78"**), a third collector region (**762"**), a third base region (**75"**) and a third base region to collector region spacing D_{Z3}, and further is adapted to have a third trigger voltage $Vt1_{Z3}$ at $D=D_{Z3}$ different than the first trigger voltage $Vt1_{Z1}$, and wherein the slope $(\Delta Vt1/\Delta D)_{Z1}$ for the first transistor (ESD-Z**1**) is greater than a slope $(\Delta Vt1/\Delta D)_{Z3}$ of the third transistor (ESD-Z**3**). According to a yet further embodiment, D_{Z3} is greater than D_{Z1}. According to a still yet further embodiment, the slope $(\Delta Vt1/\Delta D)_{Z2}$ is less than the slope $(\Delta Vt1/\Delta D)_{Z3}$. According to a yet still further embodiment, D_{Z2} is less than D_{Z1}. According to another embodiment, D_{Z1} lies in the range $1.2\text{-}1.3<D_{Z1}<2.4\text{-}2.5$ micrometers. According to a still another embodiment, D_{Z2} is equal or less than about 1.2-1.3 micrometers. According to a yet another embodiment, D_{Z3} is equal or greater than about 2.4-2.5 micrometers.

[0047] According to a second embodiment, there is provided a method for a stacked ESD clamp (**100-105**), comprising, providing a semiconductor substrate (**72**) of a first conductivity type and having an upper surface (**71**), forming at least a first transistor (**70**) having a first conductivity type first well region (**75**) extending a first distance (**751**) into the substrate (**72**) from the first surface (**71**), the first well region (**75**) having a first lateral edge (**752**) forming a portion of a base (**28**) of the first transistor (**70**), forming at least a second transistor (**70'**) having a first conductivity type second well region (**75'**) extending a first distance (**751**) into the substrate (**72**) from the first surface (**71**), the second well region (**75'**) having a second lateral edge (**752'**) forming a portion of a base (**28**) of the second transistor (**70'**), forming in the first transistor (**70**) a third well region (**927**) of a second opposite conductivity type extending a third distance (**928**) into the substrate from the first surface (**71**), the third well region (**927**) having a third lateral edge (**929**) separated from the first lateral edge (**752**) by a first spacing dimension D**1**, forming in the second transistor (**70'**) a fourth well region (**927'**) of a second opposite conductivity type extending a third distance (**928**) into the substrate from the first surface (**71**), the fourth well region (**927'**) having a fourth lateral edge (**929'**) separated from the second lateral edge (**752'**) by a second spacing dimension D**2**, and wherein the first transistor (**70**) is serially coupled to the second transistor (**70'**) and D**1** is different than D**2**. According to a further embodiment, the first spacing dimension D**1** chosen from a first zone Z**1** of spacing dimensions D, wherein the first transistor (**70**) is adapted to have a trigger voltage $Vt1_{Z1}$ and a trigger voltage slope $(\Delta Vt1/\Delta D)_{Z1}$ at D=D**1**, the second spacing dimension D**2** is chosen from a second zone Z**2** of spacing dimensions D, wherein the second transistor (**70**) is adapted to have a trigger voltage $Vt1_{Z2}$ and a trigger voltage slope $(\Delta Vt1/\Delta D)_{Z2}$ at D=D**2**, and $(\Delta Vt1/\Delta D)_{Z1}$ is at least twice $(\Delta Vt1/\Delta D)_{Z2}$. According to a further embodiment, the method further comprises providing at least two electrically isolated buried layer regions (**73**, **73'**) of a second, opposite, conductivity type spaced from the upper surface (**71**), the first buried layer region (**73**) underlying the first transistor (**70**) and the second buried layer region (**73'**) underlying the second transistor (**70'**). According to a still further embodiment, the method further comprises providing one or more deep trench isolation (DTI) walls (**792**, **792'**) electrically separating the first and second transistors (**70**, **70'**). According to a yet further embodiment, D**1** is in the range of about from 1.2-1.3 micrometers to about 2.4-2.5 micrometers. According to a still yet further embodiment, D**2** is in the range of less than or equal about 1.2-1.3 micrometers or greater than or equal to about 2.4-2.5 micrometers.

[0048] According to a third embodiment, there is provided a stacked electrostatic discharge (ESD) protection clamp (**95**, **100-104**) for protecting an integrated circuit (IC) or other circuit core (**24**), comprising, a first bipolar transistors (**70-1**, **700-1**) adapted to have a first trigger voltage $Vt1_1$ substantially determined by a first base-collector spacing D_1 of the first transistor (**70-1**, **700-1**), a second bipolar transistors (**70-2**, **700-2**) adapted to have a second trigger voltage $Vt1_2$ substantially determined by a second base-collector spacing D_2 of the second transistor (**70-2**, **700-2**) serially coupled to the first bipolar transistor (**70-1**, **700-1**), and wherein the first transistor (**70-1**, **700-1**) is adapted to have a first slope $(\Delta Vt1/\Delta D)$ of trigger voltage Vt**1** versus collector-base spacing dimension D of a first value $(\Delta Vt1/\Delta D)_1$ and the second transistor (**70-2**, **700-2**) is adapted to have a second slope $(\Delta Vt1/\Delta D)$ of trigger voltage Vt**1** versus collector-base spacing dimension D of a second value $(\Delta Vt1/\Delta D)_2$, and the first $(\Delta Vt1/\Delta D)_1$ and second $(\Delta Vt1/\Delta D)_2$, slope values differ. According to a further embodiment, the first $(\Delta Vt1/\Delta D)_1$ and second $(\Delta Vt1/\Delta D)_2$, slope values differ by at least a factor of